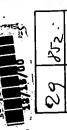
## 363 886



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PATENT NUMBER

U.S. UTILITY Patent Application

O.I.P.E.

PATENT DATE

APPLICATION NO. 09/736499 Cont/PRIOR CLASS SUBCLASS 852 ART UNIT 379 EXAMINER 134 852 ART UNIT 379 EXAMINER 134 Toshihiro Nishii Toshiaki Takenaka Shinji Nakamura

Method of manufacturing a circuit board and its manufacturing apparatus

PTO-204 12/99

	, ISSUING (	CLASSIF	ICATION				
ORIGINAL	CROSS REFERENCE(S)						
CLASS SUBCLASS	CLASS	SUBC	CLASS (ONE	SUBCL	ASS PER B	LOCK)	
129 852	29	153	830	387	<b>大小</b>		
INTERNATIONAL CLASSIFICATION	/			456	1000		
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M Q 😾			34. 1	7,93° 334	一通常		<b>***</b>
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TERMINAL		DRAWINGS		CLAIMS ALLOWED			
└─ DISCLAIMER	Sheets Drwg.	Figs. Drwg	Print Fig.	Total Claims	Print Claim for O.G.		
The term of this patent	· · · · · · · · · · · · · · · · · · ·			NOTICE OF ALLO	WANCE MAILED		
subsequent to(date) has been disclaimed.	(Assistant Examiner) (Date)						
The term of this patent shall not extend beyond the expiration date of U.S Patent. No.	Timothy V. Elev		7	7123/3			
			Ĺ	ISSUE FEE			
	_	Examiner		Amount Due	Date Paid		
		Examiner)	09/22 03	1300			
	3			ISSUE BAT	CH NUMBER		
The terminalmonths of this patent have been disclaimed.	Micelle J. (Legal Instrum	ents Examiner)	9-2503 (Date)				
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